

# KAYRA ERISOGLU-AKYILDIZ

+1(613) 884-9521 ◊ Waterloo, ON

[derisogl@uwaterloo.ca](mailto:derisogl@uwaterloo.ca) ◊ [linkedin.com/in/derin-kayra](https://www.linkedin.com/in/derin-kayra) ◊ [www.kayra.ca](http://www.kayra.ca)

## SUMMARY OF QUALIFICATIONS

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- Experienced in multiple disciplines of electrical and computer engineering with skills in microfabrication, circuit and software design.
- 5+ years of programming experience with Python, C, C++ and well versed in OOD and algorithm design.
- Proficiency with microfabrication processes with experience in cleanroom work, research cleanroom processes for semiconductor device microfabrication

## EDUCATION

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**Candidate for Honours Co-op Computer Engineering BSc**, University of Waterloo 2019 - 2024

## SKILLS

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<b>Programming</b>	C, Verilog, VHDL, C++, Python, Java, JavaScript, MATLAB, Shell scripting, SQL
<b>Microfabrication</b>	Heidelberg MLA, SEM, acid wetbenches, wire-bonding, die-bonding, dicing, spin coating, plasma cleaning, probe station
<b>Tools</b>	Cadence, Proteus, LTSpice, KiCAD, Quartus Prime, Layout Editor
<b>Mechanical</b>	Solidworks

## EXPERIENCE

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**Experimental Quantum Physics Research Assistant** Sept 2023 - Present  
Institute for Quantum Computing Supervisor: Alexandre Cooper-Roy

- Designed and built hardware and software architecture for low latency reconfiguration system integration into Rydberg quantum simulator.
- Led effort of LLRS integration into the experimental setup with team of grad and undergrad students.
- Developed and maintained LLRS while preparing for its public release and productization.

**Optoelectronic Semiconductor Devices Research Assistant** Jan 2023 - Aug 2023  
University of Waterloo Supervisor: William Wong

- Developed packaging processes for the bonding of  $\mu$ LEDs onto TFT backplanes to achieve 100% yield.
- Developed improvements for Indium electroplating growth for bonding processes to achieve successful bonding.
- Fabricated  $\mu$ LED and backplane samples using cleanroom technologies and planned new process steps for passive matrix  $\mu$ LED arrays.
- Designed new optoelectronic characterization system software to double measurement productivity.
- Created novel circuit and mechanical designs for improvements of the LED characterization system.

**Software Developer Intern** Jan 2022 - Apr 2022  
OpenText Corporation *Montreal, QC*

- Developed new software features on Spring webapp, optimizing and improving functionality of the service.
- Implemented and verified software bug fixes for Java Spring business software product.
- Authored new tests and improved existing Junit testing to increase code coverage to 80% in core projects.
- Improved and troubleshooted Maven build bugs in collaboration with team, and wrote technical documentation.

**Core Software Developer Intern** May 2021 - Aug 2021  
Kings Distributed Systems *Kingston, ON*

- Designed and implemented distributed compute protocol (DCP) worker error handling improvements.
- Initiated and organized an internal documentation effort to address a lack of developer documentation.
- Authored a DCP client web chess application with AI using a distributed minimax algorithm on the DCP platform.
- Optimized existing structures in the code base as a part of constant iterative improvement of the core product.

### **Junior Software Developer Intern**

Sept 2020 - Dec 2020

Kings Distributed Systems

*Kingston, ON*

- Implemented and designed a vital DCP scheduler microservice as defined by the specification.
- Tested and reviewed code as part of the quality assurance responsibilities of all core team dev team members.
- Collaborated on scheduler microservice design decisions with team of 5+ core developers.
- Authored fixes for existing bugs in the core codebase and created test cases for continuous integration.

### **Software Test Development Student QNX/ML**

Jan 2020 - Apr 2020

BlackBerry QNX

*Ottawa, ON*

- Built, deployed and tested team's ADAS software on 2 new hardware platforms specialized for demo purposes.
- Refined and tested scripts for software deployment, prepared documentation for demo teams.
- Performed QNX Networking benchmark test suites for QNX OS benchmarking on new hardware.
- Operated under an Agile scrum team, exercised high degrees of communication and collaboration.

## **PROJECTS**

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### **Volumetric Display**

- Designed and manufactured circuit architecture for low latency motor and display control of 3D display.
- Authored inter-device communication protocols for closed loop control of display output.
- Designed the mechanical assembly for volumetric display including motor and display housing.
- Design software system to compile 3D object files into compatible format for volumetric visualization.

### **5 Staged Pipelined RISC Processor**

- Implemented a multiply and accumulate module, and cascaded counter using Xilinx Vivado simulator and ModelSim.
- Developed a systolic matrix multiplication hardware unit to multiply to matrices of size  $M \times N$  using Verilog.
- Synthesized, deployed and debugged on a PYNQ FPGA board and optimized for maximum operation frequency.

### **Matrix Multiplier Hardware Unit.**

- Implemented a multiply and accumulate module, and cascaded counter using Xilinx Vivado simulator and ModelSim.
- Developed a systolic matrix multiplication hardware unit to multiply to matrices of size  $M \times N$  using Verilog.
- Synthesized, deployed and debugged on a PYNQ FPGA board and optimized for maximum operation frequency.

### **Real Time Operating System.**

- Developed a Binary Buddy system memory allocator and a mailbox IPC system for inter task communication.
- Built a real time task management scheduler using the earliest deadline first priority scheduling policy.
- Implemented an interactive command line interface with fully functional console I/O capabilities.

### **Distributed Web Chess Application.**

- Designed, implemented and tested a web-based chess application using the Distributed Compute Protocol.
- Developed distributed minimax and pruning algorithms to run on a distributed compute cluster with search depth of 5.
- Authored a RESTful backend API and a frontend user interface with React for a full stack web app in NodeJS.

### **Stream Cipher Encryption.**

- Created a stream ciphers program with a pseudorandom number generation algorithm and binary-to-text conversion using ASCII armour to allow for screen printable encryption.
- Included an equivalent decoder algorithm to convert ciphertext back into plaintext with a cryptographic key.
- Successfully implemented encryption for any character stream, printable or nonprintable, of variable length.