KAYRA ERISOGLU-AKYILDIZ

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EXPERIENCE

Experimental Quantum Physics Research Assistant Sept 2023 - Present
Institute for Quantum Computing Supervisor: Alexandre Cooper-Roy

- Designed and built hardware and software architecture for low latency reconfiguration system integration into Rydberg quantum simulator.
- Leaded effort of LLRS integration into the experimental setup with team of grad and undergrad students.
- Developed and maintained LLRS while preparing for its public release and productization.

Optoelectronic Semiconductor Devices Research Assistant Jan 2023 - Aug 2023
University of Waterloo Supervisor: William Wong

- Developed packaging processes for the bonding of μLEDs onto TFT backplanes to achieve 100% yield.
- Developed improvements for Indium eletroplating growth for bonding processes to achieve successful bonding.
- Fabricated μLED and backplane samples using cleanroom technologies and planned new process steps for passive matrix μLED arrays.
- Designed new optoelectronic characterization system software to double measurement productivity.
- Created novel circuit and mechanical designs for improvements of the LED characterization system.

Software Developer Intern Jan 2022 - Apr 2022
OpenText Corporation *Montreal, QC*

- Developed performance enhancing features on Spring webapp while improving Maven build processes.
- Authored new tests and improved existing Junit testing to increase code coverage to 80% in core projects.

Core Software Developer Intern Sept 2020 - Aug 2021
Kings Distributed Systems *Kingston, ON*

- Designed and implemented a vital DCP scheduler microservice in collaboration with a team of 5+ core developers.
- Designed and implemented distributed compute protocol (DCP) worker error handling improvements.

SKILLS

Programming	C, Verilog, VHDL, C++, Python, Java, JavaScript, MATLAB, Shell scripting, SQL
Microfabrication	Heidelberg MLA, SEM, acid wetbenches, wire-bonding, die-bonding, dicing, spin coating, plasma cleaning, probe station
Tools	Cadence, Proteus, LTSpice, KiCAD, Quartus Prime, Layout Editor, SolidWorks

PROJECTS

Volumetric Display • Designed and manufactured circuit architecture for low latency motor and display control of 3D display. • Authored inter-device communication protocols for closed loop control of display output. • Designed the mechanical assembly for volumetric display including motor and display housing. • Design software system to compile 3D object files into compatible format for volumetric visualization.

5 Staged Pipelined RISC Processor • Realized a 5 stage fully pipelined RISCV processor with instruction bypassing and forwarding in Verilog. • Synthesized and optimized the design on a PYNQ FPGA board.

Real Time Operating System. • Developed a Binary Buddy system memory allocator and a mailbox IPC system for inter-task communication. • Built a real time task management scheduler using the earliest deadline first priority scheduling policy. • Implemented an interactive command line interface with fully functional console I/O capabilities.

EDUCATION

Candidate for Honours Co-op Computer Engineering BASc, University of Waterloo 2019 - 2024